Inkjet Printed, High Mobility Inorganic-Oxide Field Effect Transistors Processed at Room Temperature

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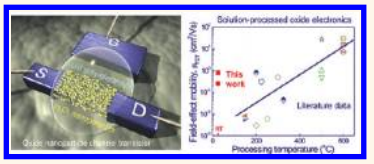
ABSTRACT Printed electronics (PE) represents any electronic devices, components or circuits that can be processed using modern-day printing techniques. Field-effect transistors (FETs) and logics are being printed with intended applications requiring simple circuitry on large, flexible (*e.g.*, polymer) substrates for low-cost and disposable electronics. Although organic materials have commonly been chosen for their easy printability and low temperature processability, high quality inorganic oxide-semiconductors are also being considered recently. The intrinsic mobility of the inorganic semiconductors are always by far superior than the organic ones; however, the commonly expressed reservations against the inorganic-based printed electronics are due to major issues, such as high processing temperatures and their incompatibility with solution-processing. Here we show a possibility to circumvent these difficulties and demonstrate a room-temperature processed and inkjet printed inorganic-oxide FET where the transistor channel is composed of an interconnected nanoparticle network and a solid polymer electrolyte serves as the dielectric. Even an extremely conservative estimation of the field-effect mobility of such a device yields a value of 0.8 $cm^2/(V\,s)$, which is still exceptionally large for a room temperature processed and printed transistor from inorganic materials.



KEYWORDS: printed electronics · inorganic oxide FET · nanoparticle channel transistor · electrochemical gating · high mobility · room temperature processing

The printing of solution-processed electronic devices[1] opens the door to massive application markets in inexpensive and large-area electronics such as in radio frequency identification tags (RFID's),[2] flexible electrophoretic displays,[3] artificial skins[4] *etc*. From the advent of the idea of solution-processed electronics, organic semiconductors have been the obvious choice due to their easy solution processability and printability.[5,6] However, after an initial rapid progress, the device mobility, achieved with completely solution processed or printed organic semiconductors, has stalled around 0.1−0.6 $cm^2/(V\,s)$.[7,8] This has been accompanied by another limitation pertinent to the applicability which is the scarcity of air-stable, nontoxic processing, n-type organic semiconductors with high mobility and performance as compared to the more abundant p-types.[9,10] In this regard inorganic semiconductors can be an alternative as most of the inexpensive, nontoxic, high quality oxide semiconductors are electron conductors. Solution-processed/printed inorganic semiconductor channel transistors can be produced from either (1) an oxide precursor, subsequently heated to obtain a high quality undoped/doped oxide semiconductor,[11−13] or (2) from a dispersion of inorganic nanoparticles as an ink (nanoink).[14−16] Up to now, the first technique has involved high temperature processing that limits the choice of substrates, which especially negates the possibility of using polymers or papers. In the latter case, one is further hindered by the difficulty to establish a smooth interface between the nanoparticulate channel and the dielectric.[14] Consequently, obtaining a satisfactory field-effect is nearly impossible when the nanoparticles are printed. In addition, the stabilizer molecules which are usually added to get stable nanoparticle dispersions remain as a semi-insulating barrier between the particles which act as charge traps and reduce mobility[15] and switching speed[16] of such devices.

Inorganic semiconductors, in general, are intrinsically far superior to the organic ones. At least 2 orders of magnitude larger intrinsic mobility ($\mu_{int} > 100\ cm^2/(V\,s)$) values are regularly observed for oxide semiconductors.[17−20] In addition, high performance FET devices

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are abundant when such oxide semiconductors are vacuum deposited. As an example, a field-effect mobility as high as 120−140 $cm^2/(V\ s)$ has been reported by the group of Marks,[21] when In_2O_3 films are prepared by ion-assisted deposition. However, disappointingly such high performance inorganic devices cannot be solution-processed at room temperature to simultaneously comply with the polymer substrates and the printing techniques. In other words, when they are solution-processed and realized at sufficiently low temperature the intrinsic performance superiority is completely lost and they even show much poorer performance when compared to the organic semiconductors.[14,15,22−24] This is primarily the reason why the oxide FETs were never really considered seriously as a contender for printed, large-area electronics.

Here, we introduce a new approach to address some of the above-mentioned shortcomings. A FET device is proposed in which a transistor channel is composed of printed inorganic oxide nanoparticles forming an interconnected network, similar to numerous `*nanopearl*' chains in parallel, and an extremely efficient gating is achieved by a solid polymer electrolyte. In itself, electrochemical gating with liquid or solid electrolyte is not a new concept. In the past few years, several groups have already reported electrochemically gated organic FETs.[7,10,25−28] However, with this very simple sounding approach we show an inkjet printed, room-temperature processed (potentially can even be realized on paper substrate) n-channel MOSFET device (NMOS) from inorganic oxide nanoparticles. The device mobility is already very similar to that reported for amorphous silicon (even when it is extremely underestimated) and still has a large potential for further improvement.

The specific advantages offered by the combination of a nanoparticulate channel and electrochemical gating are the following: (1) The advantage of using nanoparticle dispersions over oxide precursors lies in the fact that the nanoparticles used to produce the nanoink can typically be synthesized at very high temperatures and therefore can exhibit high crystallinity and large intrinsic carrier mobility.[17−20] (2) The nanoparticulate channel is inevitably quite rough. Therefore a good semiconductor−dielectric interface can only be obtained if a polymeric solid electrolyte is utilized to apply the gate voltage. As the electrolyte is liquid when added/printed, it infiltrates the nanoparticulate network and closely follows the surface roughness of the channel to create an atomically smooth interface and then slowly solidifies. Thus, with the concept of electrochemical gating an ultimate conformity between the nanoparticulate channel and the electrolyte (gate dielectric) is possible to achieve, which is believed to be the key to success in the present device type. Moreover, a high capacitance of an electrolyte ensures high gating efficiency and enables low voltage operation.

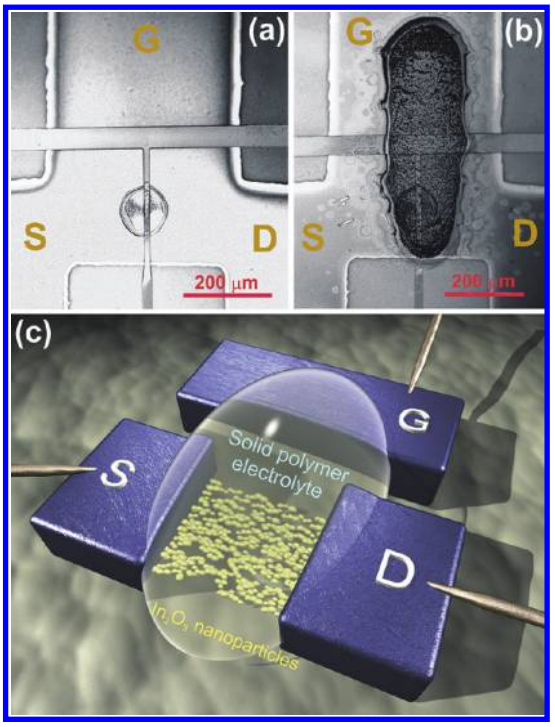

Figure 1. (a−b) Optical images of a typical in-plane In_2O_3 transistor. (a) Patterned (with e-beam lithography) passive structures from 120 nm sputtered ITO films and a printed drop of In_2O_3 nanoink. The typical device dimensions are $L \times W = 10\ \mu m \times 120\ \mu m$. (b) The optical image of the same device after printing the electrolyte. (c) A schematic presentation of the device showing highly porous nanoparticle channel which is completely infiltrated by the solid polymeric electrolyte.

RESULTS AND DISCUSSION

Presently, only the active components (channel and electrolyte) are printed, while the passive elements are prepared by conventional thin film deposition and e-beam lithography techniques. The optical images of the device are shown in Figure 1a,b and its schematic diagram is presented in Figure 1c. The prototype device is built as an in-plane transistor; the source (*S*), the drain (*D*), and the gate (*G*) electrodes being on the same plane of the substrate. The device fabrication starts with a 120 nm thick ITO (Sn-doped In_2O_3) film sputtered on poly(ethylene naphthalate) (PEN) substrate. The passive structures are made with e-beam lithography using poly(methyl methacrylate) (PMMA) as the photoresist. Then, the active FET components are printed at room temperature using a Dematix DMP 2831 inkjet printer in two subsequent steps; first the nanoparticle ink followed by the electrolyte. The nanoparticle dispersion (nanoink) of indium oxide (In_2O_3) (primary particle size ≈ 6 nm, see Supporting Information Figure S1) is printed to bridge the gap (10 μm) between the source and the drain (as shown in Figure 1a) to form the transistor channel. The

electrolyte solution is then printed to cover completely the transistor channel and partially the gate electrode (Figure 1b).

To prepare the nanodispersion for the inkjet printer, semiconducting nanoparticles (In_2O_3) and a low concentration of a weak organic base (ethanolamine or piperazine) as the surfactant is added to deionized water (solvent). To obtain the nanodispersion (nanoink), the mixture is spun in a homemade dispersion unit developed from a commercially available dissolver/mixer (DISPERMAT) with zirconia pearls as the milling media, followed by a centrifugation and finally filtration through filters of 200 nm pore size. The size distribution of the agglomerates is monitored before and after the centrifugation as well as after the filtration using transmission electron microscopy (TEM) (Supporting Information, Figure S1) and dynamic light scattering (DLS) techniques (Figure 2). The nanoinks obtained this way appear to be slightly milky (Figure 2a); the average agglomerate size in the nanoink is found to be around 20 nm (Figure 2b,c) for both the stabilizers used. It can be seen from the DLS measurements that right after the milling in the dispersing unit, there are still large agglomerates, bigger than 300 nm present in the dispersion (Figure 2b,c). However, the bigger ones are nearly eliminated with the centrifugation and when the final filtration has been performed agglomerates larger than 100 nm are no longer detected; this observation is well supported by the TEM images taken on a nanoink drop (Supporting Information, Figure S1). The high-quality and monodispersity of the agglomerates in the nanoink are essential to guarantee an easy printing with the inkjet printer; for an inkjet nozzle diameter of 21.5 μm (Dematix DMP 2831), agglomerates larger than 200 nm would clog the cartridge nozzles.[29] The stability-period of the ink is shown in Supporting Information, Figure S2, illustrating the reagglomeration tendency of the filtered ink; surprisingly, the nanoinks stabilized only with a minute amount of organic amines are found quite stable over time and hence printable over a period of months (Supporting Information, Figure S2). Although for the reported nanoparticle dispersions, which are heavily stabilized with commercially available stabilizers, long-term stability of the order of several months to even years are not uncommon, the frequently used polymeric stabilizers create a semi-insulating barrier between the particles resulting in poor electronic performance.[16] In contrast, simplest forms of primary amines ideally unite two aspects: unaltered electronic transport properties and high quality of nanodispersions which are stable over a sufficiently long period. The retained good conductivity of the ink can be due to the small size and quantity of added amines which may not cover the nanoparticles completely; thus the capillary forces acting during the drying of the nanoink may be sufficient to bring the particles to the direct physical contact and can even form a solid−solid interface.

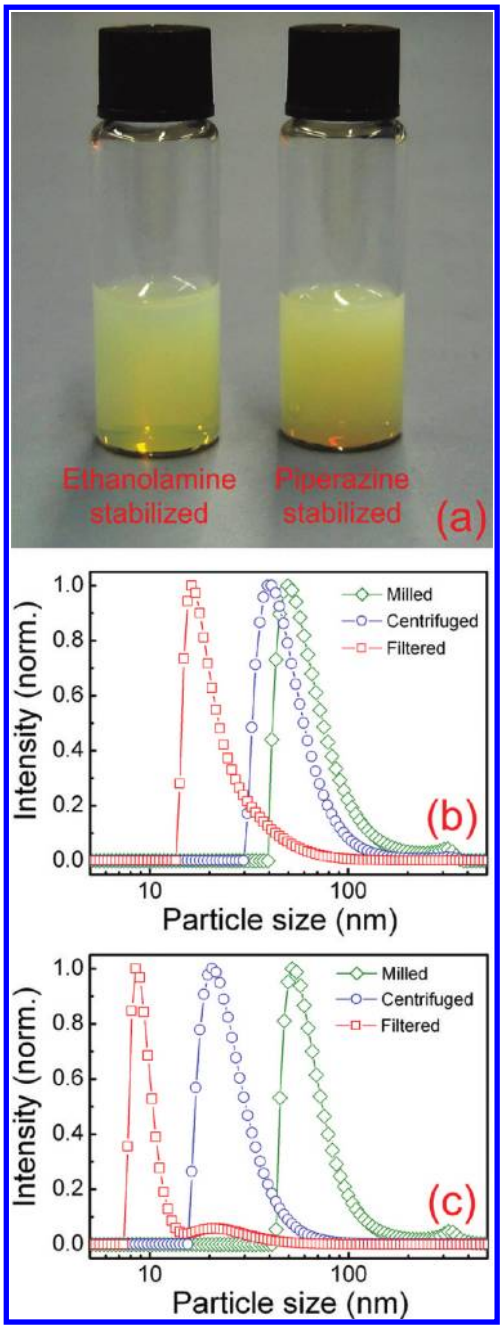

Figure 2. (a) Optical image of filtered nanoink, showing the slightly milky color of In_2O_3 nanoparticles in the dispersion, (b,c) Dynamic light scattering measurements at different stages of (In_2O_3) nanoink preparation, for ethanolamine and piperazine stabilized inks, respectively.

To facilitate the understanding of the device characteristics it has been found necessary to examine the microstructure and morphology of individual printed droplets. Identical nanoink drops are printed on a surface-treated PEN substrate and TEM grids with free-standing silicon nitride films. The scanning and transmission electron microscopy (SEM, TEM) images are shown in Figure 3. Figure 3(a−c) shows an SEM

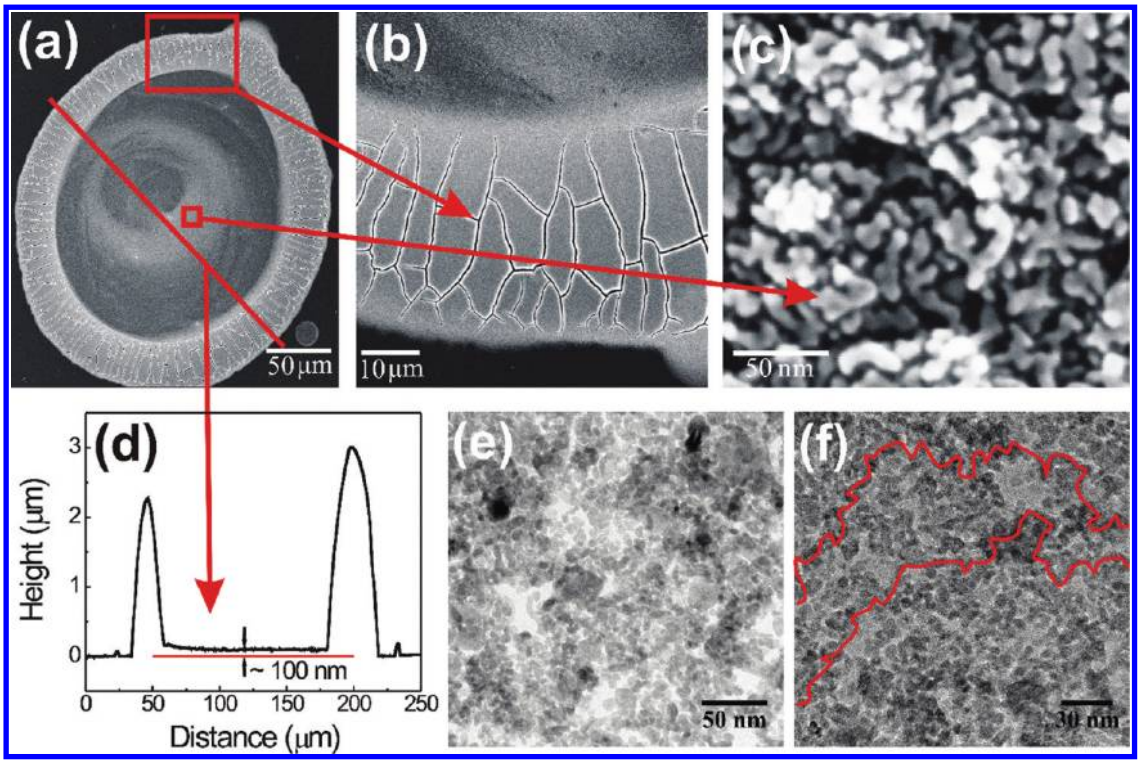

Figure 3. (a–c) SEM images of a typical printed In_2O_3 droplet on piranha cleaned PEN substrate. (a) The image shows the complete drop with coffee-ring pattern characteristic for inks with water as the solvent; (b) the enlarged image of the ring, shows high degree of cracking due to large (several micrometers in thickness) accumulation of ceramic nanoparticles; (c) image of the central area showing individual particles with some possible percolation paths. (d) Profilometric line profile of the same droplet showing a large height difference between the center and the rim of the drop. (e,f) Medium-high resolution TEM images of the central area of a similar droplet printed on the piranha-treated TEM grid with 30 nm Si_3N_4 membrane; they show similar arrangement of nanoparticles with countable percolation paths between left to right side of the image. To help the visualization of such tracks, a couple of such paths are traced with red lines.

image of a complete drop, the corner ring of the droplet, and the central area of the droplet, respectively. The complete droplet shows a ring pattern, widely known as coffee-ring effect[30] which is typical for surfactant-treated water based dispersions[31] and results from the capillary flow of solvent (water) toward the pinned edges at the perimeter which are also the evaporation maxima of the drying droplets. This capillary flow has taken a large fraction of the dispersed nanoparticles also to the outer ring as seen in the micrographs in Figure 3 and has resulted in a nanoparticulate chain-like structure at the center. As the thickness of such rings is over several micrometers (Figure 3d), they always contain numerous cracks and hence do not contribute to the electronic transport. Electron micrographs of the central region of the drop (Figure 3c,e,f), on the other hand, show an interconnected nanoparticle network, with occasional small (less than 50 nm) agglomerates. This inner region is typically made of a nanoparticulate film, mostly a few tens of nanometers in height, and the overall structure is similar to interconnected or sometimes parallel chains of nanoparticles. Possible conducting paths can be identified by following such *nanopearl*-chains. A couple of such chains (probable conducting paths), are marked in red in Figure 3f. The number of such conducting paths must be rather small in such a structure yielding a sheet resistance ($R_\square$) of such droplets over 1 GΩ. For this value of $R_\square$, an assumption of an effective thickness (solid thin film) of In_2O_3 thin film in the order of 10 nm, already leads to a resistivity of 10^3 Ω-cm, 4-to-5 orders of magnitude higher than the theoretical value for indium oxide. However, such a microstructure and high base-resistance are necessary to ensure sufficiently low OFF-current. Figure 3d shows a profilometry scan across the droplet (Figure 3a) which revealed structural features quite similar to that obtained from the electron micrographs, apart from the thickness of the film at the central region which is found to be around 100 nm. This thickness assessment by the profilometer is largely overestimated when compared to the TEM images (Figure 3e,f) where the film thickness in most areas is observed within a few tens of nanometers (one-to-few particles in height). The discrepancy may be due to the large diameter (12.5 μm) of the profiler tip which only records the highest features in the film encountered within a large distance of tens of micrometers.

The switching mechanism and transistor characteristics of a typical printed device are illustrated in Figure 4. A schematic diagram of the nanoparticle channel explains the working principle (Figure 4a);

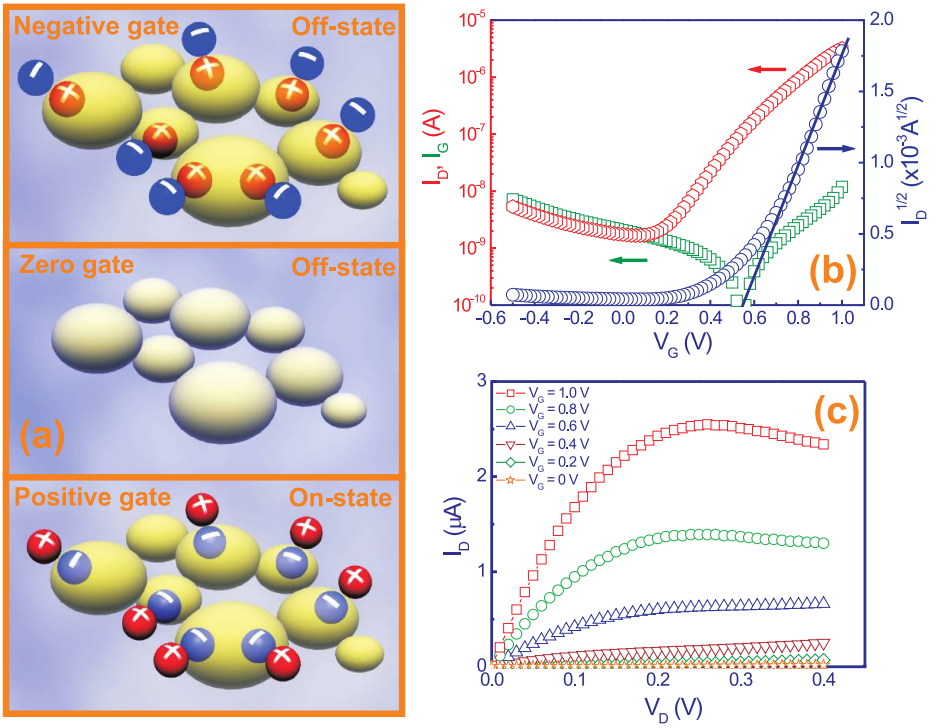

Figure 4. (a) Schematic diagrams showing the switching mechanism of an electrochemically gated nanoparticle channel transistor. (b) Transfer characteristics of the In_2O_3 nanoparticle channel and electrochemically gated transistor; the nanoink is stabilized with ethanolamine. The applied drain voltage is V_D= 0.4 V. The red prism, the blue circle and the green square represent the drain current, the square root of the drain current and the gate current, respectively. The threshold voltage (V_T) is obtained by extrapolating the linear part of the $I_D^{1/2}$ and it is found to be 0.54 V; the turn-on voltage (V_{ON}) is observed to be 0.08 V. (c) drain current–drain voltage characteristics of the same device for V_G = 0 to 1 V, with an interval of 0.2 V.

the switching of the transistor is governed by the surface charge or, in other words, electric charge double layer formed at the nanoparticle–electrolyte interface. At a negative gate voltage, the channel is positively charged; therefore, the FET channel consisting of indium oxide, an electron conductor, is in the *OFF-state*. At zero gate bias (which is equivalent to zero charge at the nanoparticle surface), the transistor is also off as there are not enough intrinsic carriers to cause a large channel conductance. Finally, the positive gate bias attracts positive ions toward the channel surface which in turn causes electron accumulation in the channel and leads to the *ON-state* of the transistor. Thus, in the operational sense, the FET is analogous to a normally off, accumulation-mode, n-channel MOSFET (NMOS). Importantly, one should also carefully exclude any chemical interference while using such a gating approach. To ensure better performance and reliability of such a device, it is necessary to guarantee that the field-effect is solely responsible for the change in channel conductance. Chemical reactions at the nanoparticle–electrolyte interface should be negligible or completely suppressed. Accordingly, chemically stable and inert materials should only be chosen to construct the channel and nonadsorbing supporting electrolytes are preferable. Thus, when the double layer capacitive window at the electrode–electrolyte interface is utilized, the process becomes analogous to a regular dielectric gating. On the other hand, use of chemically active materials or the electrolytes which prefer to adsorb on the electrode surfaces would result in a change in channel conductance due to redox/chemical reactions. These reactions should be avoided as much as possible as they would hamper long-term reproducibility of the transistor characteristics, and being kinetically rather slow, these processes would reduce the switching speed of such a device. Figure 4(b,c) shows the transfer and the current–voltage characteristics. The OFF-current is in the order of nA; a close to zero turn-on voltage (V_{ON}) and the threshold voltage (V_T) of a few hundreds of millivolts are generally observed. The applied gate voltage is limited in the present experiments to 1 V to avoid any adsorption at the nanoparticle–electrolyte interface. However, owing to the large specific capacitance/polarizability of the electrolyte used, an appreciable ON-current close to 10^{-5} ampere (W/L = 12) and ON/OFF ratio more than 2 × 10^3 is recorded. The gate current, also plotted in Figure 4b, has resulted mostly from the parasitic current of the high conducting (ITO) passive structures which are also in contact with the electrolyte (see, Figure 1b). It is clear that the "*OFF*" current of the device is limited by this parasitic capacitance of the contacts and can be reduced further with a better control over the printing process and by the top-gate device architecture. In the *I*–*V* characteristics, a phenomenon known as a *negative differential resistance*

(NDR) is always observed for every device at the large applied gate bias (mostly observed for the highest applied gate voltage of 1 V). Most likely, self-heating is not the origin of this effect as less than a microwatt is fed to the system; carrier trapping is also not an obvious reason for highly crystalline oxide semiconductors, such as In_2O_3 in the present case. However, the added surfactants (primary amines), if present between interparticle contacts, can indeed act as charge traps. Nevertheless, in contrary to this hypothesis, negligible hysteresis is observed for the transfer curves of the present device type (Supporting Information, Figure S5). Therefore, it is suggested that most likely the NDR is a result of an onset of a small adsorption process (as a result of the large drain and gate potential) at the nanoparticle surface; the same phenomenon has also been observed by other groups working with electrochemical gating.[32−34] The field-effect mobility of the device is calculated from the saturated drain current according to the equation:

$$I_{D,\,sat} = \frac{W}{2L}\mu_{FET}C(V_G - V_T)^2 \qquad (1)$$

To calculate the mobility it is necessary to know the capacitance per unit area (C) of the nanoparticles in the channel region. The true capacitance of such a droplet of the nanoink is found to be extremely difficult to measure as it is quite close to the sensitivity limit of the instrument used (*Agilent* parameter analyzer), and there is always a chance of erroneous estimation due to the current resulting from high conducting contact pads. Therefore, the double layer capacitance (DLC) of indium oxide is measured using sputter deposited In_2O_3 thin films and found to be equal to ~3.2 μF/cm^2 (Supporting Information, Figure S4); which is very similar to the value reported in the literature.[35] To be able to use the DLC from sputtered In_2O_3, to calculate the mobility of a nanoparticulate channel, it is necessary to estimate the surface area of the nanoparticulate channel in contact with the electrolyte and contributing to the channel conductance. It is clear from the HRTEM (Figure 3e,f) and AFM (Supporting Information, Figure S3) images that although the printed droplets include scattered agglomerates of the size of 40−50 nm, it is not possible to realize long enough conduction paths for a distance of even a micrometer by connecting them. Therefore, the agglomerates, although present within the channel like high-conducting islands, do not contribute effectively to the overall electrical conductivity. Therefore, considering that the conducting layer is effectively one particle in height, the channel mobility is calculated either using a flat-channel approximation (Figure 5a) which leads to a value of 0.8 cm^2/(V s), or with a nanowire network approximation where it is assumed that the particles are effectively one monolayer in height and arranged like a densely packed parallel network of nanowires without any gap in-between (Figure 5b). This arrangement of nanoparticles along with a surround gate (3-D gating) would increase the actual width of the channel by a factor of π, and hence the device mobility would be reduced to 0.26 cm^2/(V s).

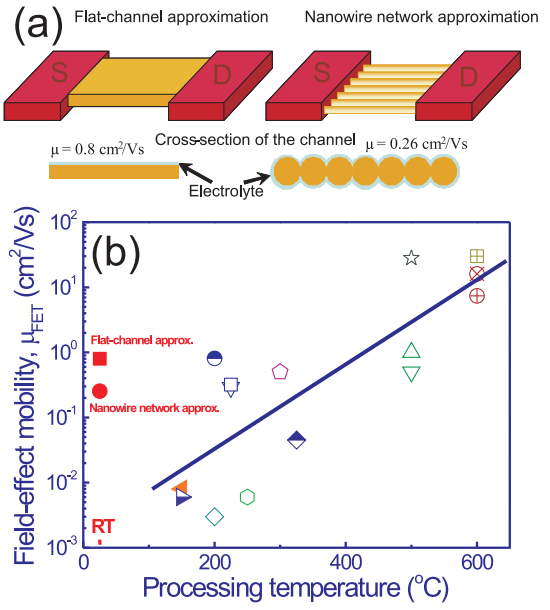

Figure 5. (a) Schematic representation of the active channel of the transistor device showing the most obvious channel geometry approximations; the respective cross-sectional view of such approximations are also shown. (b) Processing temperature versus field-effect mobility of the inorganic oxide semiconductor channel FETs from the literature; the plot includes data of both type of devices produced from oxide precursors and oxide nanoparticle dispersions, single and multicomponent oxides, crystalline and amorphous semiconductors. The open and half-filled symbols represent multi- and single component semiconductor devices from precursor route, respectively; the completely filled ones are from nanoparticle dispersions. The deep-yellow square is the data for printed IZTO,[11] maroon circles are printed and spin-coated IZO,[38] printed and spin-coated ZTO are blue star[13] and olive triangles,[39,40] respectively; pink pentagon[41] and green hexagon[12] represent spin-coated IZO and IZTO, respectively; the prism in cyan is another example of spin coated IZO.[22] The half-filled prism[23] and half-filled triangle[24] represent amorphous ZnO devices, whereas the half-filled circle is the indium oxide channel device[42] prepared from combustion synthesis. The blue open square and inverted triangle are other examples of combustion synthesized IZO and ZTO channel devices,[42] respectively. Finally the orange, filled triangle depicts the value for nanoparticle channel ZnO transistors,[15,16] and the mobility value of the transistor presented in this work is marked with red symbols (square and circle).

This calculated value of mobility of the present device is quite comparable to some of the best reported organic FETs (OFETs) that can be found in the literature.[7−10,36,37] Furthermore, among the solution-processed inorganic devices the field-effect mobility of the present FET is also considerably larger than the values reported earlier when the processing temperature is taken into consideration. Figure 5b summarizes the previously reported field-effect mobility values of solution-processed and potentially printable inorganic

TABLE 1. Details of the Materials, Process Parameters, Mobility and Dielectrics Used in Different TFT's Which Are Presented in Figure 5

transistor channel		symbols	semiconductor	processing	process temperature (°C)	mobility (cm^2/Vs)	dielectric	ref.
oxide precursors	multi-component oxides	⊞	Indium-zinc-tin oxide (IZTO)	printed	600	30	SiO_2	11
		⊠	Indium-zinc oxide (IZO)	spin coated	600	16.1	SiO_2	38
		⊕	Indium-zinc oxide (IZO)	printed	600	7.4	SiO_2	38
		☆	Zinc-tin oxide (ZTO)	spin coated	500	28	ZrO_2	13
		△	Zinc-tin oxide (ZTO)	printed	500	1	SiO_2	39
		▽	Zinc-tin oxide (ZTO)	printed	500	0.5	SiO_2	40
		⬠	Indium-zinc oxide (IZO)	spin coated	300	0.5	SiO_2	41
		⬡	Indium-galium zinc oxide (IGZO)	spin coated	250	6×10^{-3}	SiO_2	12
		◇	Indium-zinc oxide (IZO)	spin coated	200	3×10^{-2}	SiO_2	22
		□	Indium-zinc oxide (IZO)	spin coated	225	0.32	a-Al_2O_3	42
		▽	Zinc-tin oxide (ZTO)	spin coated	225	0.29	a-Al_2O_3	42
	single-component amorphous oxides	◓	In_2O_3	spin coated	200	0.81	a-Al_2O_3	42
		◆	ZnO	spin coated	325	4.5×10^{-2}	SiO_2	23
		▶	ZnO	printed	150	6×10^{-3}	SiO_2	24
oxide nano-particles		◀	ZnO	spin coated	150	8×10^{-3}	SiO_2	15,16
		■	In_2O_3	printed	25 (RT)	0.8	electrolyte (flat-channel)	this work
		●	In_2O_3	printed	25 (RT)	0.26	electrolyte (nanowire network)	this work

oxide devices with corresponding processing temperatures. Literature data for transistors produced from oxide precursors and also from nanoparticle dispersions were considered in this survey. The process parameters

and the material details of all the FETs shown in Figure 5b are listed in Table 1. From Figure 5b, one can comprehend that even though the plot includes a variety of inorganic semiconductors single- or multicomponents, crystalline, semicrystalline or completely amorphous, a characteristic correlation between processing temperature and the device mobility can be recognized. The reason has already once been mentioned in the introduction that with a lowering of the process temperature, the intrinsic high mobility of an inorganic semiconductor gets considerably reduced. Figure 5b depicts that the device mobility of the inorganic oxide FETs can be extremely high in the order of several tens of $cm^2/(V\ s)$, when the transistors are processed at elevated temperatures, such as 500−600 °C and the mobility values drop drastically with the reduction in processing temperatures. Interestingly, it is also possible to obtain a reasonable linear-fit of the literature data presented in this figure. Clearly, by the time the process temperature is lowered enough to allow inexpensive plastic substrates to be used, the oxide electronic devices show insignificant mobility (or even an absence of field-effect). In this context, the present work shows that a completely room temperature processed, inkjet printed FET with a mobility close to amorphous silicon (~1 $cm^2/(V\ s)$) is feasible with the electrochemical gating approach.

Furthermore, it is especially possible to delve deeper into the mobility calculation of our device. It has already been shown in Figure 3 that due to the use of water as the solvent and to facilitate low OFF-current, coffee-ring patterns were allowed for the printed droplets which in turn resulted in a *nanopearl*-chain-like active area and countable conducting paths that bridge drain to source. It is observed in the high-resolution transmission electron micrographs (HRTEM) (Figure 3f), that the percolation paths are particularly wavy and not many are found in a 200 nm frame (Figure 3f). This suggests that for a 10 μm channel length the number of percolation paths would be even smaller. Therefore, it can be noted that for the present device the channel length (10 μm) in eq 1 is underestimated ($L_{real} > L$) and the width (120 μm) has been completely overestimated ($W_{real} \ll W$). In other words the capacitance used in eq 1 is obtained by measuring In_2O_3 sputtered films and hence must also be extremely overestimated; that is, the DLC of the nanoparticulate layer must be much smaller than the DLC of the sputtered film used in the calculation ($C_{dl,nano} \ll C_{dl,film}$). When this argument would be true that the number of the percolation paths are extremely limited and the width of the channel is highly overestimated, the mobility calculation presented in this work (following both approximations) would clearly be an underestimation to a large extent. Therefore, it may be safe to conclude that generally for the present device-type there exists a large scope for further

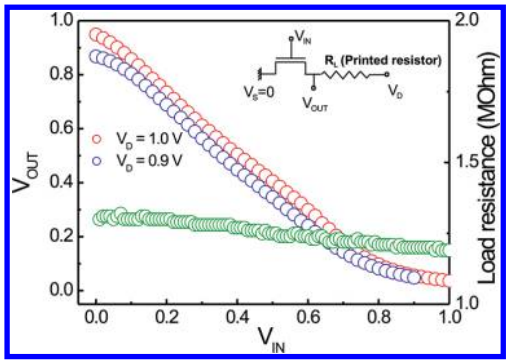

Figure 6. Demonstration of a simple logic gate (NOT gate) with one In_2O_3 transistor and one resistor (a multipass printed thick layer of In_2O_3 nanoink); the unipolar single-transistor inverter circuit is shown at the inset.

improvement in device mobility, just by following some technical modifications in order to avoid coffee-ring patterns to facilitate printing of dense and compact nanocrystalline films. Also the carrier density inside the oxide nanoparticles can be tailored by using different chemical compositions, doping with other elements, or by different annealing treatments. For example, the carrier concentration of indium oxide is extremely high (of the order of $10^{19}/cm^3$) which can easily be lowered with oxygen annealing to allow a better packing of nanoparticles while maintaining a low OFF-current. Similarly, efforts can also be directed to improve the interparticle contacts to increase the FET mobility further. Following the reported device mobility of 175 $cm^2/(V\ s)$ by J. Sun *et al.*[43] for electrolyte-gated single-crystalline oxide semiconductor channel transistor, we believe that the electrochemical gating of semiconducting inorganic oxide nanoparticles, in principle, can provide an extremely large value of device mobility, when an improved physical and therefore electronic structure of the FET channel is achieved.

Additionally, technological improvements of the printing techniques would eventually bring down the smallest printed feature-size; however, scaling of an electrochemically gated FET device in order to obtain smaller channel lengths is always possible without a hindrance imposed by the short channel effects.[44] For an electrochemical gating, the applied gate voltage decays within the thickness of the charge double layer, which is (except for very dilute electrolytes) not much larger than the thickness of the Helmholtz layer and only about one to a few nanometers wide.[45] Consequently, scaling of the channel lengths down to 100 nm or even less would still show the saturation of a drain current.[46] Thus, in the case of a nanoparticle-channel device where the building blocks of the channel are nanoparticles which are several nanometers across, the advantage of suppressed short channel effects offered by the electrolyte gating approach can further differentiate this technology from others.

In the next step a simple printed logic is demonstrated in Figure 6; it shows the transfer curve of a

unipolar single-transistor NOT gate (voltage inverter) where both the transistor channel and the load (resistor) are printed using an indium oxide nanoink. The output of the inverter shows a gain not much larger than one (peak gain ~1.4), which is probably due to the fact that the transistor is operating mostly within the linear regime (see, transfer characteristics, Figure 4b) when the gate potential is limited to 1 V. However, most importantly the simple printed logic operates under one volt and shows the correct logic function. On the other hand, a larger gain can easily be obtained either by larger applied voltage (V_{IN} and V_D), increasing the width of the channel, putting several devices in parallel or by a complementary (CMOS inverter) circuit design. Application of a larger bias in an inverter circuit should not be a problem because the input (V_{IN}) and the drive (V_D) voltages are never simultaneously large at the active element.

CONCLUSIONS

In summary, a prototype device and a new method to prepare a printed n-channel MOSFET from a nanoink containing inorganic oxide semiconductor nanoparticles are presented. The simple and inexpensive concept described in this work shows a process to fabricate an inkjet-printed and completely room-temperature processed inorganic channel FET with a significantly higher device mobility compared to the values reported in the literature and a big potential for further improvement using a systematic engineering development. To the best of our knowledge, this is the first demonstration of an inorganic transistor printed on a flexible substrate and processed at room temperature. The low gate voltage (≤1 V) requirement for such an electrochemically gated device makes it battery-compatible and adds to its merit to enhance the application potential.

METHODS

Nanoink Preparation. To prepare the nanoparticulate ink, 10 wt % of indium oxide nanopowder (Plasmachem GmbH) was added to deionized water (solvent) which was loaded with 0.1 wt % of stabilizer (weak organic bases, such as ethanolamine or piperazine) and a certain amount of zirconia pearls (200−300 μm) (milling material). The mixture was spun for 90 min with a rotational speed of 9000 rpm in a homemade dispersing unit based on commercially available dissolver/mixer called DISPERMAT, followed by a centrifugation (Eppendorf, Centrifuge 5415D). Prior to the centrifugation the zirconia pearls are separated by filtering through a 5 μm syringe filter. The supernatant of the centrifuged nanodispersion was collected carefully leaving the bigger agglomerates at the bottom of the capsule, and then the dispersion was finally filtered through a 200 nm PVDF membrane filter to obtain the nanoink. The size distribution of the agglomerate diameter was measured with transmission electron microscopy (TEM) (FEI TITAN) (Supporting Information, Figure S1) and dynamic light scattering (DLS) (ALV-NIBS High Performance Particle Sizer) (Figure 2). The nanoparticle loading in the nanoink thus obtained was calculated by evaporating the solvent and found around 2 wt %.

Electrolyte Preparation. The electrolyte, which is a polymeric solid electrolyte, consists of a water-soluble synthetic polymer, polyvinyl alcohol (PVA) of low molecular weight (degree of polymerization 300, saponification 98%), deionized water as the solvent, and a nonadsorbing supporting electrolyte, such as potassium fluoride (KF). Equal amounts of PVA and KF were added to deionized water separately and homogenized with constant stirring at 75 °C. The clear solution of KF was then added to the viscous PVA solution and stirred until the complete solution becomes entirely homogeneous. The KF concentration in the electrolyte was usually kept low (~0.1 M). It was found from the mass balance experiment performed on the dried electrolyte (at the ambient conditions) that even after drying it still contains 30% of water[47] which is responsible for the high conductivity (2.5×10^{-2} Scm^{-1}) in such composite polymer electrolytes.[48]

Printing. The printing was performed with commercial Dematix DMP 2831 inkjet printer with piezoelectric nozzles with nozzle diameter of 21.5 μm. All the printing steps were carried out at room temperature on precleaned and lithographically structured 125 μm thick polyethylene naphthalate (PEN) substrates. The PEN substrate (DuPont) was cleaned with piranha (75% concn H_2SO_4, 25% H_2O_2) solution. The as-received free-standing Si_3N_4 membrane TEM grids were significantly hydrophobic; therefore, to create identical surface condition the TEM grids with 30 nm Si_3N_4 membrane (Agar scientific) were similarly cleaned in piranha. Using the same printing parameters (printing voltage and waveform) on such grids as compared to the PEN foils resulted in identical fluid flow and similar drop size and morphology which in turn ensured that the piranha treatment created a similar surface energy of the grids and the PEN substrates.

Characterization. The height and morphology of the printed layer were characterized by profiling with a Dektak 6M stylus profiler with the N-Lite low force package (Veeco). The nanoparticle arrangement/distribution in the printed area on PEN films was investigated with a Leo 1530 Gemini scanning electron microscope (SEM), and similar printed areas on TEM grids with a free-standing silicon nitride membrane were examined with a transmission electron microscopy (TEM) using a FEI Titan 80-300 microscope.

Electrical Measurements. The electrical measurements were performed at room temperature and in ambient conditions. For contacting the electrodes a precision probe station (SUSS MicroTec MLC-150C) was used. The electrical measurements were carried out with a precision semiconductor parameter analyzer (Agilent 4156C).

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Supporting Information Available: Additional figures contain medium-high and high-resolution TEM images of the nanoink and individual indium oxide nanoparticles, DLS measurements showing the long-term stability of the indium oxide nanoinks, atomic force microscopy images showing the particle distribution and morphology of the printed droplets, double layer capacitance (DLC) measurement of sputtered In_2O_3 thin films and hysteresis in the printed In_2O_3-channel MOSFETs. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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